Patent Claims

1. A method for testing an integrated memory having a main data memory with a plurality of data memory units, comprising:

a) addressing a data memory unit by applying an address of the data memory unit to an address bus operably coupled to the main data memory;

b) applying input test data to a data bus operably coupled to the main data memory to test the addressed data memory unit;

c) reading out output test data from the addressed data memory unit;

d) comparing the output test data with expected desired output test data;

e) storing the applied address, the expected desired output test data, and the output test data as information in a redundancy analysis memory if a deviation of the output test data from the desired output test data occurs;

f) providing first redundant areas in the redundancy analysis memory and providing at least second redundant areas outside the redundancy analysis memory; and

g) determining a repair strategy by means of the first and second redundant areas on the basis of the information stored in the redundancy analysis memory.

2. The method of Claim 1, further comprising dividing the main data memory, for testing purposes, into sub-areas that are tested separately.

3. The method of Claim 2, wherein dividing the main data memory comprises dividing the main data memory into sub-areas of identical size or of different size, and determining a repair strategy for each sub-area,

the testing of the entire main data memory being carried out in an iterative manner by the sub-areas being tested one after the other.

4. The method of Claim 2, wherein the first redundant areas of the redundancy analysis memory is provided for repairing each sub-area and the at least second redundant areas are provided for only one sub-area in each case.

5. The method of Claim 1, wherein at least one first sub-area of the main data memory is provided as a redundant area.

6. The method of Claim 5, wherein the first sub-area is firstly tested and, after successful conclusion of the testing of the first sub-area, transferring useful information items of a sub-area that is to be tested as a further sub-area to the first sub-area.

7. The method of Claim 1, further comprising employing the first redundant areas, depending on the number of detected deviations of the output test data from the expected desired output test data before the at least second redundant areas of the integrated memory for the determination of the repair strategy.

8. The method of Claim 7, further comprising exclusively employing first redundant areas of the redundancy analysis memory for the repair strategy if a test run is ended and a storage capacity of the redundancy analysis memory is occupied at most maximally with information items of the defective data memory units detected.

9. The method of Claim 1, wherein determining the repair strategy in accordance with step g) further

comprises the following if the storage capacity of the redundancy analysis memory is exceeded by the number of defective data memory units detected, that are stored in the redundancy analysis memory, and a first test run is not yet concluded:

h) reading out of the information items stored in the redundancy analysis memory into a computing unit;

i) determining an intermediate repair strategy in the computing unit by means of the at least second redundant areas;

j) continuing the first test run if the first test run is interrupted before step h); and

k) repeating steps a) to j).

10. The method of Claim 9, further comprising repeating step k) until identifying that the integrated memory is no longer repairable during or after the carrying out one of steps a) to j), or completing the test run and the storage capacity of the redundancy analysis memory after completion of the test run is occupied at most maximally with information items of further defective data memory units detected.

11. The method of Claim 10, further comprising, after completing the test run, determining a final repair strategy using previously determined intermediate repair strategies and first redundant areas and/or at least second redundant areas.

12. The method of Claim 10, further comprising altering the previously determined intermediate repair strategies during a determination of a further intermediate repair strategy or of a final repair strategy.

13. The method of Claim 9, wherein the information items stored in the redundancy analysis memory are read

out progressively or completely and transferred into the computing unit, and written from the computing unit to the redundancy analysis memory again during the determination of an intermediate repair strategy.

14. The method of Claim 9, wherein, before the execution of step i), identifying an exact defect position in the output test data by comparing the output test data with the desired output test data in the computing unit on a bit-by-bit basis.

15. The method of Claim 1, wherein the information items as to which first redundant areas and/or which second redundant areas and/or are utilized for an intermediate repair strategy or a concluding repair strategy, and the information therein are written to memory registers operably coupled to the computing unit.

16. The method of Claim 1, further comprising executing a plurality of test runs with identical or different test algorithms or, after an interruption of a single test run, a test algorithm for testing is chosen that is identical to or different from the test algorithm with which the testing is carried out before the interruption of the single test run.

17. The method of Claim 16, wherein different test algorithms are used for identifying differently categorized defects such as bit-oriented defects and word-oriented defects.

18. The method of Claim 1, wherein a first test run is executed with a maximum clock frequency of the integrated memory.

19. The method of Claim 1, wherein during the reading out of the information items stored in the redundancy analysis memory, the clock frequency with which the integrated memory is tested is reduced.

20. The method of Claim 1,

wherein a data width of a first redundant area comprises an interval which extends from a single bit up to a number of bits forming an entire word; and

wherein a data width of a second redundant area comprises an interval that extends from a single bit up to a number of bits forming an entire row or a plurality of rows, or an entire column or a plurality of entire columns.

21. The method of Claim 1, further comprising executing the repair strategy and after the repair of the integrated memory, writing the information items of the activated first redundant areas and/or the second redundant areas to a non-volatile, programmable memory.

22. The method of Claim 1, further comprising identifying defects in the second redundant areas that are used for an intermediate repair strategy, and replacing the second redundant areas with other second redundant areas and/or first redundant areas.

23. The method of Claim 1, further comprising combining the method with test methods that use error-detecting and error-correcting codes.

24. An integrated memory, comprising:

a plurality of data memory units arranged in a memory cell array;

a plurality of row lines and column lines, the plurality of row lines having regular and redundant row

lines and the plurality of column lines having regular and redundant column lines, respectively;

a self-test unit operable, in the event of an access to a row line, to check the contents of a selected data memory unit for the correctness of data therein and operable to store information items associated therewith;

a redundancy analysis memory comprising first redundant areas, the redundancy analysis memory operably coupled to the self-test unit and the information items of non-correct data memory units being stored therein;

second redundant areas arranged outside the redundancy analysis memory; and

a computing unit operably coupled to the self-test unit and the redundancy analysis memory, the computing unit operable to determine a repair strategy based on the information items stored in the redundancy analysis memory.

25. The integrated memory of Claim 24, further comprising an algorithm unit operably coupled to the self-test unit and the computing unit and operable to select test algorithms.

26. The integrated memory of Claim 24,

wherein a data width of a first redundant area comprises an interval that extends from a single bit up to a number of bits forming an entire word; and

wherein a data width of a second redundant area comprises an interval that extends from a single bit up to a number of bits forming an entire row or a plurality of rows, or an entire column or a plurality of columns.

27. The integrated memory of Claim 24, wherein the integrated memory comprises a main data memory that is

subdivided into a plurality of sub-areas, and at least one first sub-area is provided as a redundant area.

28. The integrated memory of Claim 27, wherein the second redundant area is designed as a redundant row or redundant column, or a further redundant area is designed as a sub-area of the main data memory.